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Single-Phase Grid-Forming Strategy with Power Decoupling Implementation for Electrolytic-Capacitor-Free EV Smart Battery Charger

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Abstract: Smart Battery Chargers (SBCs) implementing grid-forming (GFM) control strategies are a promising solution to provide voltage and frequency support, increasing the grid reliability. Typically, GFM studies consider inverters with high DC-link capacitance. Therefore, there is a research gap in two-stage DC-AC converters with small DC-link capacitance implementing GFM strategies. This article proposes a novel approach to implement a GFM control strategy along with active power decoupling (APD) in an isolated, single-phase, electrolytic-capacitor-free two-stage DC-AC structure. The structure is composed of a voltage source inverter (VSI), DC-linked by film capacitors, with a dual-active-bridge series-resonant (DABSR) DC-DC converter. High DC-link ripple is allowed and managed by the APD. Hence, electrolytic capacitors are avoided, increasing the converter lifetime. In the proposed approach, the VSI implements the GFM strategy, operating in the four quadrants of the active and reactive power plane. However, the DABSR allows galvanic isolation, average DC-link voltage control, and suppression of the low-frequency ripple on the battery current, minimizing the impact in the battery lifetime. Design criteria are given for the DC-link voltage controller, active-reactive power controllers, inner inverter controllers, and APD technique. The control strategy is validated for vehicle-to-grid and stand-alone vehicle-to-home applications, using hardware-in-the-loop for a 2kW test setup.

Keywords: grid-forming (GFM); active power decoupling (APD); DC-link ripple; electric vehicles (EV); Smart Battery Charger (SBC); vehicle-to-grid (V2G); vehicle-to-home (V2H)

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1. Introduction

1.1. Motivation

The use of electric vehicles (EVs) is expected to considerably increase in the coming years, progressively replacing internal combustion engine vehicles. However, a bottleneck to high EV penetration is the concern about reliability of low-voltage distribution networks with large numbers of plug-in EV which can substantially increase the peak load and potentially generate voltage regulation infringements [1]. The EV Smart Battery Charger (SBC) interfaced with single-phase grid, where active and reactive power are controlled in the four quadrants of the power plane for frequency and voltage support, has been presented as a potential solution to minimize the impact of the EV in the distribution grid, which is commonly known as vehicle-to grid (V2G) support [2]. The implementation of other modes of EV use, like vehicle-to-home (V2H) for stand-alone applications [3,4] has also increased the costumer interest for SBC. In this operation mode, the EV acts as a storage backup to supply energy to loads when the grid energy is interrupted.

However, additional challenges are required to be solved for the single-phase SBC, in particular, increasing its durability. Moreover, the single-phase SBC for EVs entails requirements such as galvanic isolation to ensure safety and low leakage currents [5] and single-phase power decoupling, which is required to decrease the low frequency ripple (LFR) in the battery current, minimizing its detrimental effect in the battery lifetime [6].

The most commonly used structure in single-phase SBCs is the isolated two-stage DC-AC converter composed of a voltage source inverter (VSI), DC-linked with an isolated and bidirectional DC-DC converter [7]. Typically, electrolytic capacitors with high capacitance values are placed in the DC-link, allowing single-phase power decoupling [8]. However, the usage of electrolytic capacitors in the DC-link carries out several disadvantages such as limited lifetime and operating temperature range, considerable volume and weight, and high price. In contrast, film capacitors have better features and overcome those disadvantages, although with the drawback of having less capacitance value [8]. Therefore, different solutions have been proposed to replace the electrolytic capacitors by film capacitors in single-phase two-stage DC-AC converters with the aim of increasing the converters lifetime [9–11]. Nevertheless, in most of these solutions, the single-phase power decoupling is presented in conjunction with active power control only, whereas SBC requires also reactive power control for voltage support [2].

According to the literature review, the studies for active and reactive power control for single-phase SBCs have been presented for two-stage DC-AC converters composed of a voltage source inverter (VSI) cascaded with a non-isolated bidirectional boost converter [2,12,13] or cascaded with an isolated Dual-Active-Bridge (DAB) DC-DC converter [14], using electrolytic capacitors with high capacitance value in the DC-link, which reduces their useful lifetimes. A three-port non-isolated DC-AC converter for V2G and photovoltaic panel-to-grid (PV2G) considering reactive grid power support and single-phase power decoupling is proposed in [15]; however, for V2G applications, galvanic isolation is highly recommended [5]. In almost all these studies, V2G support has been implemented using a grid-following (GFO) control strategy which cannot work in stand-alone V2H mode. With the aim of overcoming this limitation, an additional AC voltage control strategy with an anti-islanding algorithm must be implemented [3,4]. Hence, additional studies are required to implement V2G with active and reactive grid power support and stand-alone V2H in isolated two-stage DC-AC converters electrolytic-capacitors-free.

With the aim of covering the research gap, this article proposes a novel approach to implement a single-phase electrolytic-capacitor-free SBC for V2G support and stand-alone V2H applications using a unified grid-forming (GFM) control strategy. Only V2G and stand-alone V2H modes are analyzed in this article due to the limited power in single-phase SBCs, in addition to being the most common applications for SBCs. The analyzed structure is an isolated two stage DC-AC converter composed of a voltage source inverter (VSI) cascaded with a dual-active-bridge series-resonant (DABSR) DC-DC converter. Both stages are DC-linked by film capacitors to increase the converter lifetime. High DC-link ripple is allowed and managed by the proposed active power decoupling (APD). In the proposed control approach, the VSI implements the GFM control strategy with voltage and frequency droops, operating in all four quadrants of the active and reactive power plane in such a way that V2G and stand-alone V2H services can be performed. The DABSR DC-DC converter allows galvanic isolation, average DC-link voltage control, and active power decoupling to suppress the LFR on the battery current. The high frequency (HF) current is minimized in the DABSR DC-DC which reduces power losses in the converter. Hence, the proposed structure, along with the proposed GFM control strategy and active power decoupling, are a good candidate for EV SBC with V2G and V2H functionalities.

1.2. Literature Review

It is well known that, for a two-stage single-phase DC-AC converter, as shown in Figure 1, the instantaneous grid power is given by:

$$p_o(t) = v_{pcc}\, i_o = P_o - P_o cos\left(2\omega_g t\right), \tag{1}$$

where P_o and ω_g are the average power and the grid frequency respectively. Note in (1) that p_o has the DC component (P_o) and a low-frequency time-variant component $P_o cos\left(2\omega_g t\right)$ which oscillates at $2\omega_g$ rad/s. If this low-frequency component is not filtered in the DC-link,

a high LFR will be present in the battery current, I_i. This high LFR decreases the lifetime of lithium batteries [6].

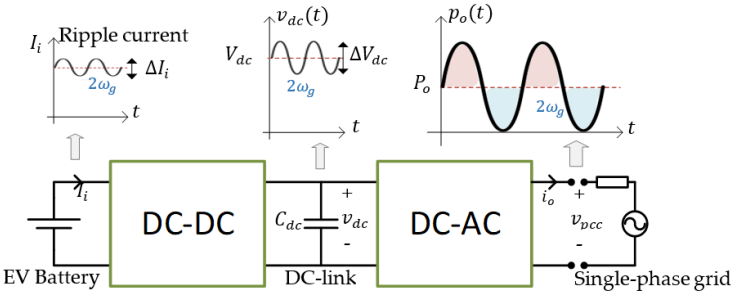

Figure 1. Instantaneous power for single-phase two-stage DC-AC converter.

According to Figure 1, considering an average DC link voltage V_{dc} and a maximum ripple ΔV_{dc}, the DC-link capacitance C_{dc} value can be estimated as [8]:

$$C_{dc} \approx \frac{S_o}{\omega_g V_{dc} \Delta V_{dc}}, \tag{2}$$

where S_o is the nominal power. Note in (2) that the C_{dc} value is inversely proportional with respect to V_{dc} and ΔV_{dc}. The DC-link capacitance value is calculated for $S_o = 2$ kVA and $\omega_g = 2\pi(60)$ in Table 1 for two cases of V_{dc} and ΔV_{dc}.

Table 1. DC Link comparison for passive decoupling considering $S_o = 2$ kVA and $\omega_g = 2\pi 60$.

Parameter	DC Link Capacitance Value	Capacitor Technology
$V_{dc} = 380$ V; $\Delta V_{dc} = 3\%$	$C_{dc} = 1.2$ mF	Electrolytic
$V_{dc} = 450$ V; $\Delta V_{dc} = 11\%$	$C_{dc} = 240$ µF	Filmic

When electrolytic capacitors are used in the DC-link, lower voltage V_{dc} and ripple ΔV_{dc} are considered for the selection of the capacitance value which allows it to filter the LFR. This method is known as passive power decoupling [8]. In contrast, when film capacitors are used in the DC-link, higher voltage V_{dc} and ripple ΔV_{dc} are considered for the selection of the capacitance value. However, even if the film capacitor usage allows the obtaining of higher durability in the converter, the high ripple in the DC-link increases the LFR in the battery current affects the battery durability. Therefore, different techniques with and without additional circuitry have been proposed to filter the LFR in the DC-link [8–11,16–23]. Of all these techniques, the most cost-effective is to replace the electrolytic capacitor with film capacitors in the DC-link, without additional circuitry with the limitation of having a high DC-link ripple [8]. Therefore, power decoupling with additional circuitry is not covered in this article.

Indeed, in two-stage DC-AC converters, the capacitance value can be decreased allowing high values of ΔV_{dc} and V_{dc}, and film capacitors can be used in the DC-link. However, the high DC-link ripple will have an impact in MOSFET stress, as well as in the grid and battery currents performance. The MOSFET stress caused by the increased voltage in the DC-link can be solved using SiC MOSFET. The influence of the high DC-link ripple on the grid current can be attenuated using a feedforward with a proportional multi-resonant controller [23]. Finally, with the aim of suppressing the LFR in the battery current, an APD must be implemented on the DC-DC converter as proposed in [20–22]. However, it should be highlighted that all the isolated two-stage DC-ACs with high LFR in the DC-link found in the bibliography have been focused on GFO control strategies [8,20–23] and not the GFM control strategy.

Additionally, an SBC that offers V2G and stand-alone V2H functionalities is presented in [3,4], switching between GFO control for V2G mode and voltage source control for

stand-alone V2H mode. Hence, two different control strategies are used to perform V2G and V2H modes, and an anti-islanding algorithm must be implemented to switch between grid-connected mode and islanding mode [4]. However, both control strategies can be replaced by a unified GFM control strategy to work in grid-connected or stand-alone mode, as presented in [24–30], making the control strategy easier to implement. The GFM control strategies have high potential to implement V2G and V2H services in EV SBCs; however, very few studies have been conducted on single-phase GFM control strategies. Among them, in [31], a GFM control strategy has been proposed for SBCs which is based on the well-known swing equation, and internally a double voltage-current loop with PR controllers is set. A droop control-based GFM strategy, also with a double voltage-current loop with PR controllers, has been reported in [32]. In [33], an approach with an internal single-loop current controller and current limitation is proposed. However, in these three studies, the DC-link voltage is considered as an infinite power source and practical implementation issues such as power decoupling with high DC-link ripple have not been covered.

Additional studies are required to implement GFM control strategies for single-phase SBCs considering the impact of the high DC-link ripple and the power decoupling. This issue has been introduced by the authors in [34] using a similar GFM control to that proposed in [31], whereas in [35], it is shown that the swing equation can operate as a PLL-free GFM control strategy. However, that proposal has been tested only for three-phase DC-AC converters but not for single-phase converters. Hence, this article modifies the PLL-Free GFM control proposed in [35] for implementation in a bidirectional and isolated two-stage DC-AC for EV SBCs considering a high DC-link ripple. The analyzed converter is composed of a single-phase VSI DC-linked by film capacitors with a DABSR DC-DC converter.

1.3. Contributions

The main contributions of this article are the following:

- Unlike typical GFM studies, where inverters using electrolytic capacitors on the DC Link with high capacitance values and small DC-link ripple are considered, this article proposes a novel approach to implement a GFM control strategy in an isolated single-phase DC-AC converter considering a high DC-link ripple and smaller DC-link capacitance values, intended for electrolytic-capacitor-free EV SBCs. The proposed GFM control strategy provides voltage and frequency support in grid-connected operation (V2G mode) and stand-alone operation to supply energy to islanded loads (V2H mode), obtaining high-quality power in both terminals (grid and battery), even in the presence of high DC-link ripple.
- A novel power decoupling for a DABSR DC-DC converter is introduced. In the proposed strategy the phase-shift angle controls the average DC-link voltage while the duty-ratio angle compensates for the high DC-link ripple. The proposed power decoupling mitigates the LFR on the DC current. The proposed modulation obtains minimal HF current and ZVS mode in the DABSR DC-DC converter. Therefore, high efficiency can be obtained.

1.4. Organization

This article is divided into the following sections: Section 2 introduces the converter structure where the modulation for the DABSR DC-DC converter is detailed. The unified single-phase GFM control with enhanced dynamic and stationary response is explained in Section 3. The power decoupling and the DC-link voltage control implemented in the DABSR DC-DC are explained in Section 4. Experimental hardware in the loop results are shown in Section 5. A comparison between the proposed single-phase GFM control along with APD strategy versus alternatives control strategies reported in the bibliography is explained in Section 6. Finally, conclusions are drawn and presented in Section 7.

2. Converter Structure

The analyzed two-stage DC-AC structure and the overall control overview are depicted in Figure 2. The two-stage DC-AC converter is composed of a VSI (DC-AC stage) cascaded with a DABSR (DC-DC stage) converter, considering a high LFR in the DC-link.

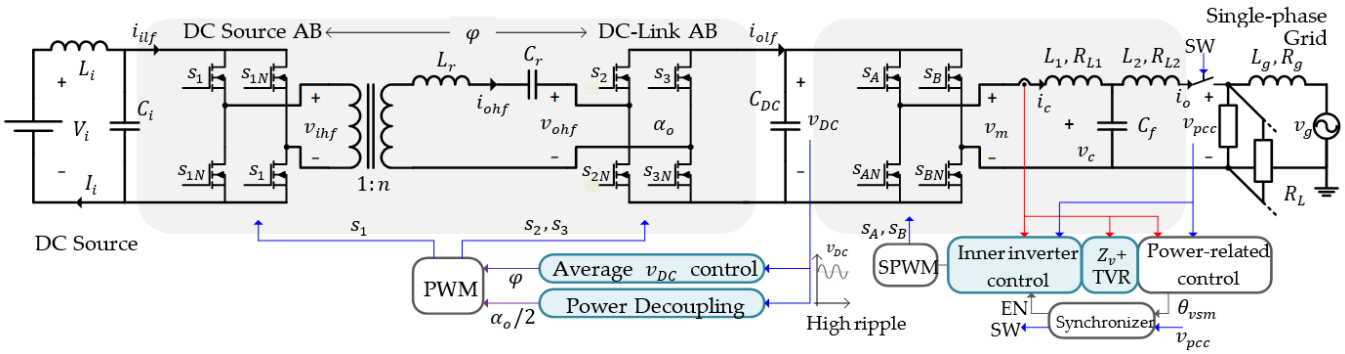

Figure 2. Two-stage DC-AC charger structure and control overview.

2.1. Voltage Source Inverter Stage

Unipolar sinusoidal pulse width modulation (SPWM) is employed for the VSI, and an LCL filter is used to attenuate the switching frequency harmonics with reduced size. A converter-side inductor is chosen to mitigate i_c current ripple, whereas a grid-side inductor is sized to improve the quality of the current injected into the grid [36,37]. The capacitance C_f value is chosen with a minimum value to minimize the impact in the current i_c and to enable the approximation $i_c \approx i_o$ for the control strategy.

At the DC-link terminal, LFR is allowed to enable the use of long-lifetime film capacitors. According to (2) and considering the values indicated in Table 1, DC-link capacitance value $C_{dc} = 240$ µF is calculated considering $V_{dc} = 450$ V and $\Delta V_{dc} \approx 49$ V. This LFR is also addressed through control for optimal performance at both terminals of the two-stage converter.

2.2. Dual-Active Bridge Series-Resonant Stage

The DABSR DC-DC converter performs the average DC-link voltage control and the APD. For this purpose, the modulating signal presented in Figure 2 are as follows:

For the DC-source Active Bridge (AB):

$$s_1 = sgn(\sin(\omega_s t - \varphi)), \tag{3}$$

For the DC-link AB:

$$\begin{cases} s_2 = sgn\left(\cos\left(\omega_s t - \frac{\alpha_o}{2}\right)\right) \\ s_3 = sgn\left(\cos\left(\omega_s t + \frac{\alpha_o}{2}\right)\right) \end{cases}, \tag{4}$$

where ω_s is the switching frequency, and the function $sgn(x)$ is defined as:

$$sgn(x) = \begin{cases} 1, & x \geq 0 \\ 0, & x < 0 \end{cases}, \tag{5}$$

The modulated voltages are shown in Figure 3. Note that two command signals are used: the duty ratio (DR) angle α_o and the phase-shift (PS) angle φ. Hence, from the Fourier Series expansion, the fundamental components of the modulated voltages of Figure 3 can be expressed as presented in (6).

$$\begin{cases} v_{ihf,1} = \frac{4}{\pi} V_i \sin(\omega_s t - \varphi) \\ v_{ohf,1} = \frac{4}{\pi} V_{om} \sin \omega_s t \end{cases}; \; V_{om} = v_{dc} \sin \frac{\alpha_o}{2} \tag{6}$$

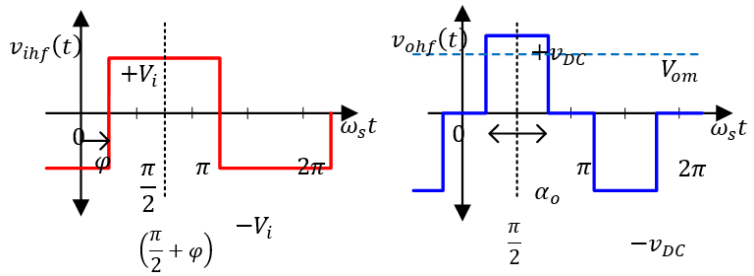

Figure 3. DABSR DC-DC converter modulated voltages.

The time-variation of v_{dc} can be considered constant during one switching period since $\omega_s \gg 2\omega_b$, where ω_b is the grid frequency. Note in (6) that V_{om} is affected by the DC-link voltage v_{dc}, which is time-variant a cause of the high ripple ΔV_{dc}, and the DR angle $\frac{\alpha_o}{2}$. In the proposed modulation, the voltage V_{om} is controlled, in open loop, to have a constant value throughout the grid period.

On the other hand, with the aim of having high selectivity at the switching frequency ω_s, the tank circuit inductance and capacitance, L_r and C_r are sized considering a high-quality factor $Q \approx 4$ and a resonance frequency ω_r close to ω_s ($\omega_s \approx 1.1\ \omega_r$) [38]. These parameters are defined as:

$$Q = \frac{Z}{\frac{8n^2}{\pi^2}\frac{V_i^2}{P}}; \quad \omega_r = \frac{1}{\sqrt{L_r C_r}}; \quad Z_r = \sqrt{L_r/C_r}, \tag{7}$$

where Z_r is the characteristic impedance of the tank circuit, n is the turns-ratio of the high frequency (HF) transformer, and P the nominal power.

To analyze the impact of LFR in the battery current, calculate the average input non-filtered current $\left\langle i_{ilf} \right\rangle$ in the DABSR DC-DC converter (see Figure 2) in one switching period as follows:

$$\left\langle i_{ilf} \right\rangle = \frac{1}{2\pi}\int_0^{2\pi} \left[n i_{ohf} \times s_1 \right] d(\omega_s t), \tag{8}$$

where s_1 is defined in (3). Since the LC filter on the battery side, shown in Figure 2, is sized to filter the switching frequency, then it is possible to make the equivalence $I_i \cong \left\langle i_{ilf} \right\rangle$. Solving (8), the battery current results in:

$$I_I \cong \left\langle i_{ilf} \right\rangle = K v_{dc} \sin\frac{\alpha_o}{2} sin\varphi = K V_{om} \sin(\varphi) \tag{9}$$

where V_{om} is defined in (6), and the constant K given by:

$$K = \frac{8n}{\pi^2 Z(F - 1/F)}, \quad F = \frac{\omega_s}{\omega_r} \tag{10}$$

On the other terminal, the average output non-filtered current $\left\langle i_{ilf} \right\rangle$ (presented in Figure 2) is calculated in a similar way as for $\left\langle i_{ilf} \right\rangle$ for one switching period, obtaining:

$$\left\langle i_{olf} \right\rangle = I_{o\varphi} \sin\frac{\alpha_o}{2}, \quad I_{o\varphi} = (K_o)\sin\varphi \tag{11}$$

In (11), $K_o = KV_i$, with K defined in (10), and V_i is the DC source voltage. Additionally, the HF transformer turns-ratio is sized as:

$$n = V_{om}/V_i, \tag{12}$$

with the aim of matching the controlled voltage on the HF transformer secondary side V_{om} with the DC source V_i. This minimizes the HF current in the series-resonant circuit, as will

be explained in the control strategy in Section 4. The two-stage DC-AC converter elements are summarized in Table 2 for a 2 kW prototype.

Table 2. Converter parameters.

Symbol	Parameter Description	Value
S_b	Nominal apparent power	2000 VA
V_b	Nominal RMS voltage	220 V
ω_b	Nominal grid angular frequency	$2\pi(60)$ rad/s
f_s	VSI and DAB switching frequency	20 kHz
L_1, C_f, L_2	LCL filter elements values	2 mH, 4.7 µF, 0.3 mH
L_g	Grid infinite bus model inductance	1.5 mH
C_{dc}	DC-link film capacitance	240 µF
ΔV_{dc}	Peak-to-peak DC-link voltage ripple	50 V
V_{dc}	Average DC-link voltage	450 V
V_{om}	Minimum DC-link voltage	380 V
Q	Series-resonant circuit quality factor	4
L_r, C_r	Series-resonant circuit elements values	1800 µH, 39nF
n	HF transformer turns-ratio	380/400
L_i, C_i	Battery filter	0.5 mH, 120 µF
V_i	Battery voltage	400 V

3. DC-AC Control: Single-Phase GFM with Improved Stability

The proposed single-phase GFM control, implemented at the DC-AC stage, is designed in a per unit (p.u.) system [39]. As shown in Figure 4, this is organized in three main levels: the power-related control, the virtual impedance, and the inner inverter control [40].

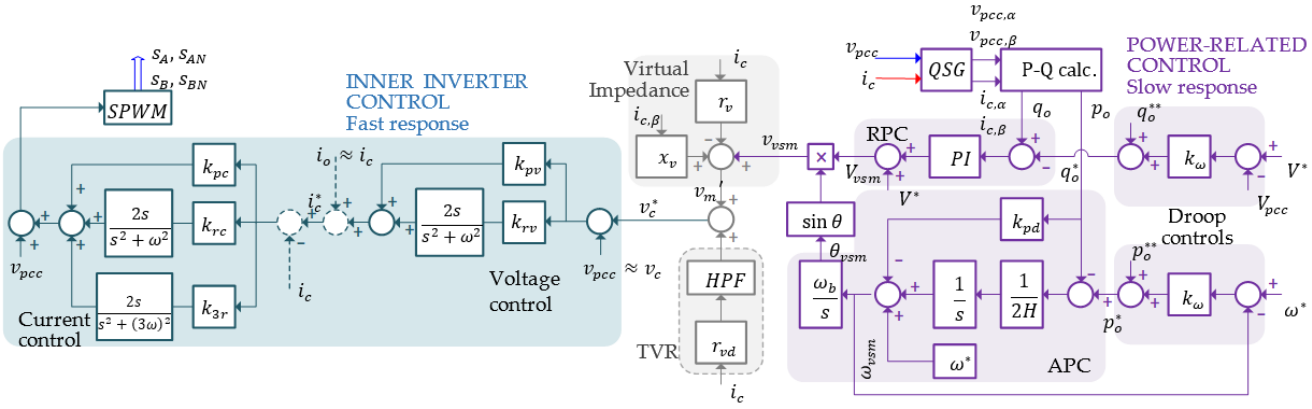

Figure 4. Proposed single-phase GFM control with improved dynamic response.

3.1. Power-Related Control

The GFM control presented is intended to operate in both grid-tied and islanded modes, but this implies two different line impedances and therefore different dynamics. Nevertheless, as discussed in [30] for dual-loop-controlled GFM converters with an LCL output filter, the control bandwidth decoupling between AC voltage and power loops is worse in a grid-tied operation in comparison to an islanded operation. When the generic power-related control is designed considering the critical case, it means it is a grid-tied operation.

The circuit model for the grid-tied converter is shown in Figure 5, where the source $V_{vsm}\angle\theta_{vsm}$ represents the VSM emf; $V_{pcc}\angle\theta_{pcc}$ is the voltage in the PCC,]; $V_g\angle\theta_g$ is the grid voltage; and z_v, z_c, and z_g are the virtual impedance, the inverter filter impedance, and the grid impedance, respectively.

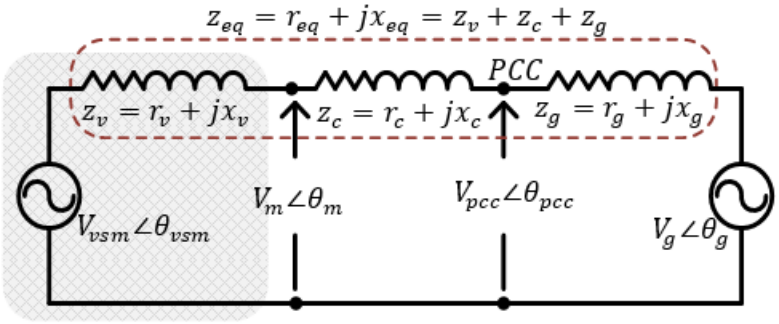

Figure 5. Model of VSM connected to the grid by a mainly inductive line.

Considering an inductive line in Figure 5, the p.u. total reactance $x_{eq} = (x_g + x_c + x_v)$ is much greater than the p.u. total resistance $(r_g + r_c + r_v)$, where $x_c = \omega_b L_1 / Z_b + \omega_b L_2 / Z_b$ is the sum of the per unit filter reactances of the converter. If the power angle $\Delta\theta = \theta_{vsm} - \theta_g$ and the voltage difference $V_{vsm} - V_g$ are small, then the approximate expressions of the active and reactive power are as presented in (13) and (14), from which it can be seen that a mainly inductive line decouples the control of active and reactive power [41]:

$$P \approx \frac{V_{vsm} V_g}{x_{eq}} \Delta\theta, \tag{13}$$

$$Q \approx \frac{V_{vsm}(V_{vsm} - V_g)}{x_{eq}}, \tag{14}$$

3.1.1. Droop Control

According to the P-Q decoupling expressed in (13) and (14), frequency and amplitude droops are implemented as presented in (15) and (16), respectively, to enable parallel operation with other VSGs and SGs and load sharing (see Figure 4). At their outputs' active power and reactive power control references, p_o^* and q_o^* are set according to the frequency and amplitude deviations in v_{pcc}:

$$p_o^* = p_o^{**} + k_\omega(\omega^* + \omega_{pcc}), \tag{15}$$

$$q_o^* = q_o^{**} + k_V(V^* + V_{pcc}), \tag{16}$$

where, p_o^{**}, q_o^{**}, ω^*, and V^* are the input references set by the charger's user. According to the nominal power of the designed converter, it is established that it must provide frequency support by injecting 4.2% of its nominal power (in W) for every 0.1 Hz reduction in v_{pcc} frequency, or by injecting 4.5% of its nominal power (in VAR) for every volt reduction in v_{pcc} amplitude, similar to [31]. Thus, the droop gains $k\omega$ and kV are set to 0.04 (4%) and 0.1 (10%), respectively.

3.1.2. Active Power Control

The mechanical part of the SM is implemented in a block that incorporates the small signal model of the swing equation, setting $\omega^* = 1\ p.u.$ as the frequency operation point as shown in Figure 4 [34]. Directly from Newton's second law for rotary motion that relates the electrical and mechanical torque in a SM, results of the swing equation are expressed in terms of electrical and mechanical powers:

$$\omega_r = \frac{1}{2H\,s}\left(p_o^* - p_o - k_d(\omega_r - \omega_{pcc})\right), \tag{17}$$

where ω_r represents the angular frequency of the SM rotor in electrical rad/s, H is the inertia constant, and k_d is the damping factor for a frequency deviation in the PCC.

For active power control (APC), the PLL-free grid forming presented in [35] is taken as reference, since it allows the tuning of its parameters setting a desired bandwidth, based on a second order model of the equivalent simplified swing equation:

$$\omega_{vsm} = \frac{1}{2H\,s}(p_o^* - p_o) - k_p p_o, \tag{18}$$

For tuning effects, the simplified swing equation model is treated as an IP controller. For a plant based on an approximation of the power sharing dependent on the angle difference $\Delta\theta$ in the two-source converter-grid model [35], this is shown in Figure 6.

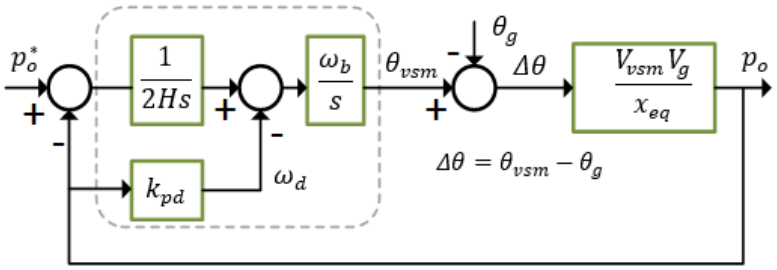

Figure 6. Block diagram for APC tuning.

According to Figure 6 and considering that the grid frequency is practically constant, the second order model for the active power is given by:

$$\frac{p_o(s)}{p_o^*(s)} = \frac{1}{\frac{2H\,x_{eq}}{\omega_b}s^2 + 2Hk_p s + 1}, \tag{19}$$

for the second-order system presented in (19), the following design conditions are established: bandwidth $BW_P = 2\pi(5)$ rad/s and damping coefficient $\zeta = 0.7$.

3.1.3. Reactive Power Control

For reactive power control (RPC), PI controller is used, which offers a stiff regulation of the reference voltage amplitude to get a certain desired reactive power [42]. Like APC, the plant for the linear model results from the approximation of the reactive power flow in inductive lines for the two-source converter-grid model, but in this case, considering the impedances instead of only reactances, performs a zero-pole elimination for tuning the PI gains. For the plant model, the approximation of the nominal voltage presented in [42] is employed. Based on these considerations, the RPC loop is as shown in Figure 7.

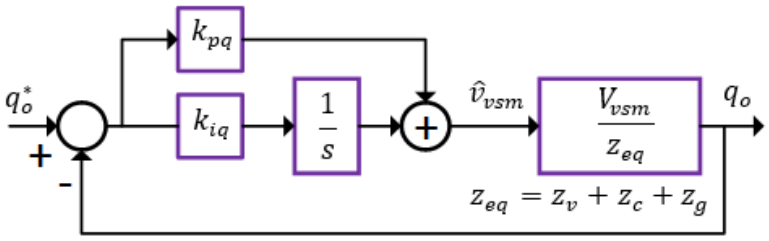

Figure 7. Block diagram for RPC tuning.

The PI controller gains k_{pq} and k_{iq} are established to set an open-loop transfer function cutoff frequency with a similar speed than the active power, $\omega_{cq} = 2\pi(5)$ rad/s.

3.2. Virtual Impedance and Stability Improvement

The active and reactive power controllers are tuned based on a linearized static model of the AC system expressed in (13) and (14), which neglects the P-Q coupling under the condition that the transmission line between the two sources is mainly inductive ($X \gg R$).

To ensure that condition, a virtual impedance z_v that emulates the stator impedance of a physical synchronous machine is implemented, generating a bandwidth reduction in power control. The virtual impedance produces a voltage drop in the VSM machine EMF (v_{vsm}), then the reference voltage at the output of the virtual impedance block is:

$$v'_m = v_{vsm} - i_c z_v; \qquad z_v = r_v + j\omega_{vsm} x_v, \tag{20}$$

To avoid noise amplification due to voltage drop in the virtual reactance requiring a derivative of the current, quasi-stationary approximation is employed, as described in [43], using the quadrature current $i_{c,\beta}$ from the power measurement block. In that way, the output reference voltage results in:

$$v'_m = v_{vsm} - i_c r_v + \omega_{vsm} i_{o,\beta} x_v, \tag{21}$$

A typical reactance value of 0.3 p.u. is chosen for x_v, as in a grid-connected synchronous machine [44]. To set and inductive stator impedance, virtual resistance is chosen following $r_v < x_v/5$.

Stability Improvement Using Transitory Virtual Resistance

Although the linear static model is a good approximation for $\Delta\theta < 30°$, it hides fast dynamics that can affect the stability of smaller AC systems. As explained in [45] for an AC system as the one shown in Figure 5, the dynamics analysis around the operation point reveals that the relations between the variation of the active and reactive powers (Δp_o and Δq_o), with respect to the amplitude and phase variations of the voltage at the output of the active bridge (ΔV_m and $\Delta\theta_m$), share the same second-order characteristic polynomial in Laplace domain:

$$\begin{bmatrix} \Delta p_o \\ \Delta q_o \end{bmatrix} = \begin{bmatrix} \frac{N_1}{D(s)} & \frac{N_2}{D(s)} \\ \frac{N_3}{D(s)} & \frac{N_4}{D(s)} \end{bmatrix} \begin{bmatrix} \Delta\theta_m \\ \Delta V_m \end{bmatrix}, \tag{22}$$

where N_1, N_2, N_3 and N_4 are second-order polynomials, and $D(s)$ is the characteristic polynomial:

$$D(s) = \left(\frac{x_{eq}}{\omega_{pcc}} s + r_{eq} \right)^2 + \left(\omega_{pcc} x_{eq} \right)^2, \tag{23}$$

the polynomial $D(s)$ shows that the oscillatory modes of the converter-grid AC system are mainly dependent of the line impedance, whose damping coefficient is:

$$\zeta_{AC} = \frac{r_{eq}}{\sqrt{r_{eq}^2 + \left(x_{eq}\omega_{pcc} \right)^2}}, \tag{24}$$

In the case that ζ_{AC} results are too small that the system is prone to destabilization, then the addition of a virtual damping resistance r_{vd} in series with the physical filter impedance may stabilize the AC system, damping the resonance peaks. Hence, the addition of r_{vd} virtually in series with the filter resistance r_c establishes a new characteristic polynomial $D^*(s) = \left(x_{eq}s/\omega_{pcc} + \left(r_{eq} + r_{vd} \right) \right)^2 + \left(\omega_{pcc} x_{eq} \right)^2$ that allows the selection of a desired new damping value ζ^*_{AC}. Then the virtual damping resistance will be designed according to:

$$r_{vd} = \frac{\zeta^*_{AC} \left(x_{eq}\omega_{pcc} \right)}{\sqrt{1 - \left(\zeta^*_{AC} \right)^2}} - r_{eq}, \tag{25}$$

However, the addition of r_{vd} affects the low-frequency response of the AC system, and therefore the model used by the P-Q controllers. To avoid this effect, a high-pass filter (HPF) must be added in series, conforming the Transitory Virtual Resistor (TVR) as shown in Figure 4, whose cutoff frequency must be less than the frequencies at which the AC system could resonate: $\omega_{c,HPF} \leq \omega_g/2$ [45]. The dynamics enhancement for three values

of ζ_{AC} in the grid-tied operation of the designed system is shown in the time-domain simulations presented in Figure 8. In islanded operation, the addition of the TVR improves the converter stability in low passive damping conditions, i.e., very low or no load is connected at the PCC.

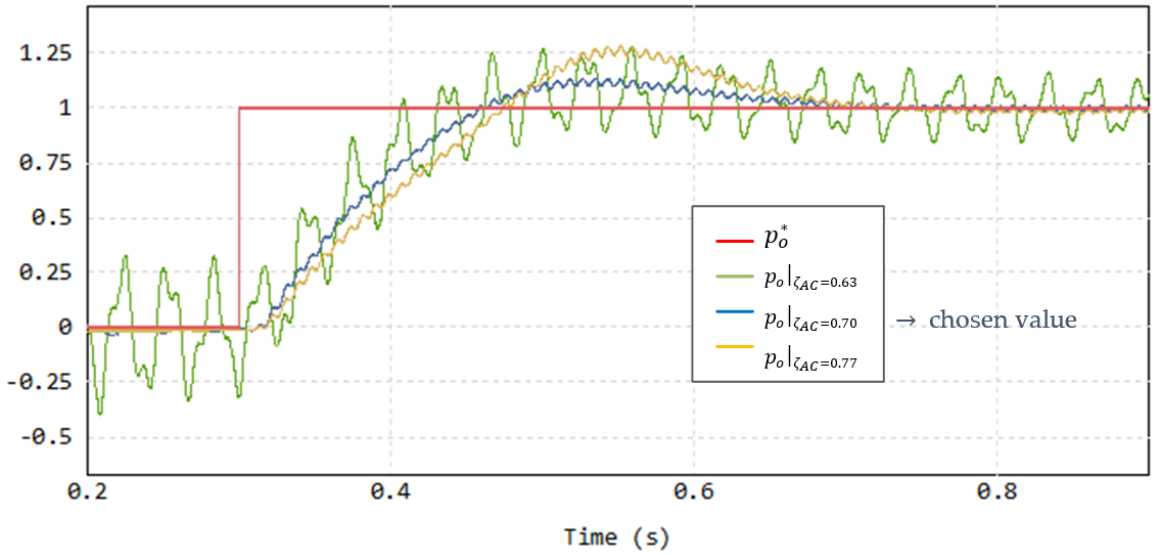

Figure 8. Active power response for 1 p.u. step under three different damping ζ_{AC} conditions.

3.3. Inner Inverter Control

The system is capable of operating without an inner inverter control, using directly v_c^* as the modulating signal in SPWM block. However, due to the use of small DC-link film capacitors, the high double-line frequency ripple (DLFR) in v_{dc} leads to high THD in the current injected into the grid. This fact makes it advisable to use a dual loop control capable of attenuate the main harmonic components of the injected current. Therefore, a dual control loop of voltage and current is incorporated as the most internal loop, and therefore the fastest of the designed system. Its reference signal v_c^* comes from the TVR.

To reduce the sensors number, the smaller capacitance C_f is chosen to approximate $i_c \approx i_o$, and the voltage drop on the grid-side inductor is neglected allowing the approximation of $v_{pcc} \approx v_c$.Then, the inner voltage controller gains are tuned considering the approximations for i_o and v_{pcc}, taking the filter capacitor $\left(C_f\right)$ as the plant and using the symmetrical optimum method to maximize the phase margin [34]. Then, the open-loop bandwidth set by the cutoff frequency $\omega_{cv} = 10\omega_b$ is chosen to calculate k_{pv} and k_{rv}, resulting in a phase margin equal to 59° for its open-loop transfer function. In addition, compensation feedforwards are added to enhance the signal tracking and to compensate external disturbances in both the voltage control loop and current control loop, as explained in [34].

The inner current control loop model is presented in Figure 9. However, for implementation, as shown in Figure 4, signal feedback (i_c) can be bypassed since it is canceled by the compensation feedforward signal ($i_o \approx i_c$), thus avoiding feeding back the signal with higher THD and related stability problems [30]. A multi-resonant controller $\mathrm{P} + \mathrm{R}_\omega + \mathrm{R}_{3\omega}$ is used to control i_c and obtain zero error in a steady state [46]. This controller is chosen due to the high presence of the third harmonic, which appears due to the high DLFR in the DC-link. Given the DC-link voltage $v_{dc}(t) \approx V_{dc} + 0.5\,\Delta V_{dc}\cos(2\omega_b t - \theta)$ and the generated PWM voltage $v_m \approx (m v_{dc})\sin(\omega_b t - \theta)$, where m is the modulation index, then the third harmonic appears as indicated in (26):

$$v_m = mV_{dc}\sin(\omega_b t - \theta) + \frac{m\Delta V_{dc}}{4}\sin(\omega_b t - \theta) + \frac{m\Delta V_{dc}}{4}\cos(3\omega_b t - 2\theta), \quad (26)$$

it can be appreciated that oscillations at $\omega_b = 2\pi(60)$ rad/s and at $3\omega_b$ are noticeable and resonant controller at ω_b and at $3\omega_b$ are required to obtain zero error in steady-state response.

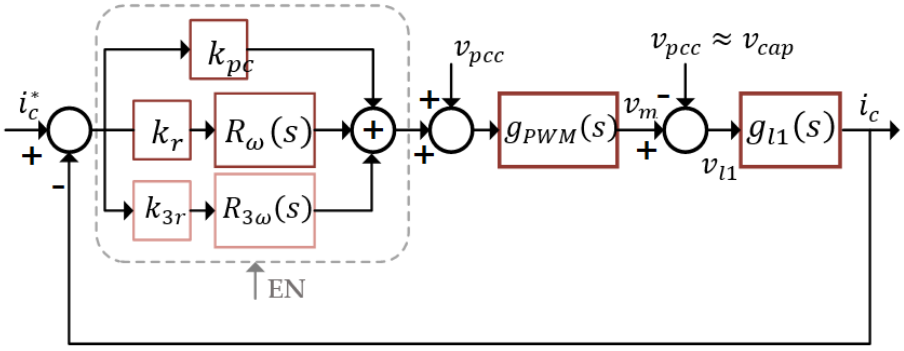

Figure 9. Inner current loop control strategy.

In Figure 9, $R_\omega(s)$ and $R_{3\omega}(s)$ are the resonant controllers centered at the frequencies $\omega_b = 2\pi(60)$ and $3\omega_b$, $g_{PWM}(s)$ represents the delay generated by modulation sampling, and the plant $g_{l1}(s)$ comes from the converter-side inductor. The tuning of the controller PR_1 is performed with its equivalent PI controller in a synchronous reference frame [47,48] to get to a desired bandwidth. By performing a zero-pole elimination and setting a cutoff frequency $\omega_{cc} = 5\omega_{cv}$, the controller gains k_{pc} and k_r are obtained.

Since the reference current given by the voltage controller has very low harmonic distortion, a resonant controller centered at $3\omega_b$ is added to track/reject the third harmonic component in the AC output current. In this case, the gain k_{3r} is selected equal to three times k_r since it achieves a high gain in the peak at $3\omega_b$, without modifying the bandwidth and phase margin. The frequency response of the open loop transfer function for the inner current control loop $g_{cc}(s)$ is shown in Figure 10.

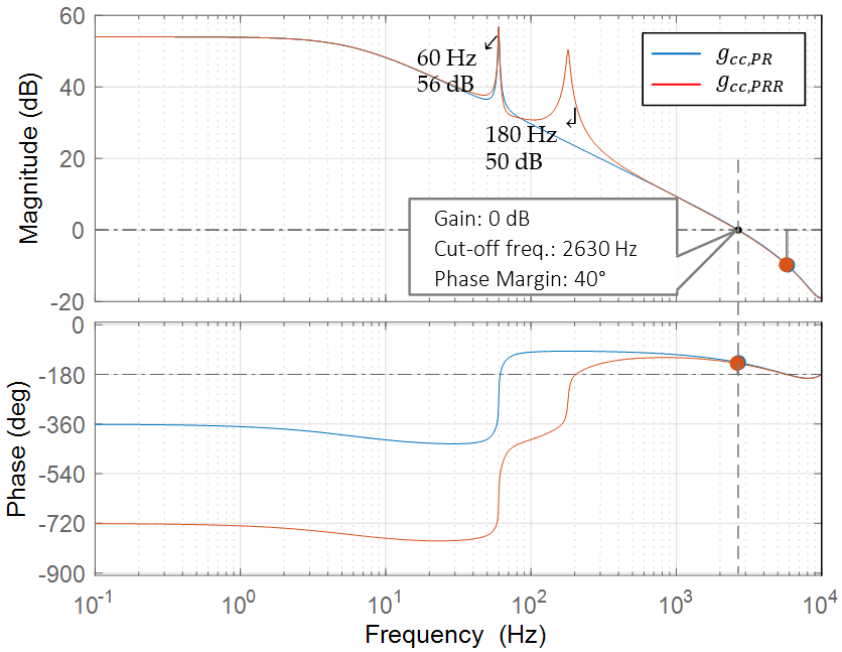

Figure 10. Bode diagram of current control open-loop transfer function $g_{cc}(s)$. Same bandwidth for P+R_1 controller (blue), and for P+R_1+R_3 controller (red).

In Figure 9, the modulating signals are disabled while the synchronization process takes place with the signal 'EN'. This action avoids integrator saturation and keeps the output voltage and current at zero during initialization.

4. DC-DC Control: DC-Link Control and Active Power Decoupling

In the proposed control strategy, the average DC-link voltage is controlled by the DC-DC converter and not by the DC-AC as is usual in GFO control strategies [20,49]. Therefore, the average DC-link voltage control along with the APD algorithm are shown in Figure 11.

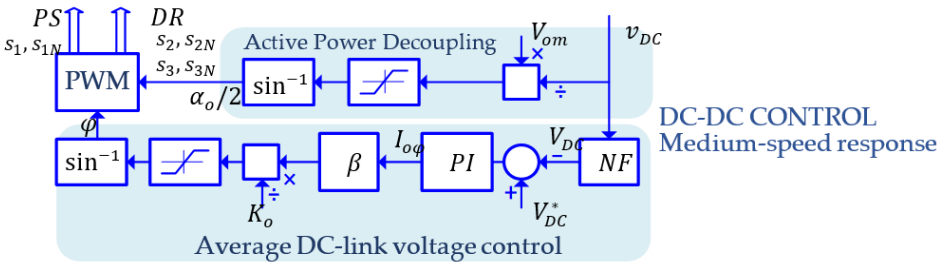

Figure 11. DC-DC average v_{dc} control with active power decoupling.

4.1. Active Power Decoupling Based on DR Modulation

The expression (9) implies that if no power decoupling is performed and considering that $\sin(\varphi)$ does not present low frequency variations, the LFR on v_{dc} will be reflected in the battery current I_i. Hence, in the proposed APD, the DR angle $\alpha_o/2$ changes in such a way that V_{om} takes a constant value in all the grid period. For this purpose, according to (6), the DR angle is calculated as follows:

$$\frac{\alpha_o}{2} = \sin^{-1}\left(\frac{V_{om}}{v_{dc}}\right) \tag{27}$$

which implies the restriction $v_{dc} \geq V_{om}$. Applying (27) in (9), the LFR of v_{dc} will be canceled in the battery current I_i since V_{om} is a set constant.

Furthermore, the HF current is expected to have a constant value amplitude throughout the grid period compared to systems that do not employ the proposed APD algorithm, since the voltage seen in the DC-link side by the resonant circuit is reduced to V_{om}. In that way, according to (6) and (27):

$$i_{ohf}(t) = \frac{4}{\pi X_r}[nV_i\cos(\omega_s t - \varphi) - V_{om}\cos(\omega_s t)], \tag{28}$$

where $X_r = X_{L_r} + X_{Cr} = Z_o(F - 1/F)$ is the total reactance of the resonant circuit. Hence, from (28) the peak value of the HF current can be estimated according to:

$$I_{ohf,\,pk} = \frac{4}{\pi X_r}\sqrt{V_{om}^2 + (nV_i)^2 - 2nV_iV_{om}\cos\varphi} \tag{29}$$

The DC-link side power can be calculated as follows:

$$P_o = v_{dc}\left\langle i_{olf}\right\rangle = KV_iV_{om}\sin\varphi, \tag{30}$$

showing that, whenever $\sin(\varphi)$ is free of low-frequency ripple, the APD algorithm decouples the low-frequency oscillations in both DABSR terminals.

4.2. DC-Link Voltage Control

In the proposed control strategy, the average DC-link voltage V_{dc} is controlled by the DABSR DC-DC converter. For this purpose, the average DC-link voltage model is shown in Figure 12, where $\left\langle i_{olf}\right\rangle$ is given by (11).

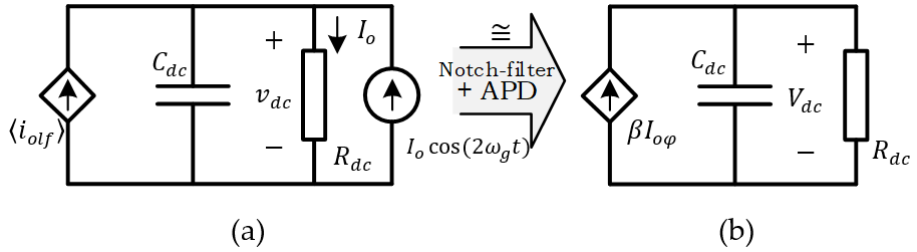

Figure 12. DC-link model: (**a**) Model considering the high LFR, (**b**) Average model with APD.

In Figure 12a, the VSI input current i_{dc} has a low frequency component $I_o \cos(2\omega_g t)$ and a DC component I_o, which means:

$$i_{dc} = I_o + I_o \cos(2\omega_g t), \tag{31}$$

where $I_o = V_{dc}/R_{dc}$, whereas $R_{dc} = {V_{dc}}^2/P_o$; R_{dc} is the output load at nominal power P_o, V_{dc} is the average DC-link voltage, and C_{dc} is the DC link capacitor. Then, according to (11) and (27), $\langle i_{olf} \rangle$ is given by:

$$\langle i_{olf} \rangle = I_{o\varphi} \sin\frac{\alpha_o}{2} = I_{o\varphi}\left(\frac{V_{om}}{v_{dc}}\right) = I_{o\varphi}\left(\frac{V_{om}}{V_{dc}\left(1 + \frac{0.5\Delta V_{dc}}{V_{dc}} cos(2\omega_g t)\right)}\right), \tag{32}$$

where V_{om} is controlled by the DR angle α_o according to (6), and V_{dc}, ΔV_{dc} are the averaged DC-link voltage and ripple, respectively. Hence, considering $1 \gg 0.5\Delta V_{dc}/V_{dc}$, the DC component of $\langle i_{olf} \rangle$, $\langle i_{olf} \rangle_{dc}$ can be rewritten as:

$$\langle i_{olf} \rangle_{dc} = \beta I_{o\varphi}, \quad \text{where } \beta = \left(\frac{V_{om}}{V_{dc}}\right), \tag{33}$$

resulting in the average model of the average DC-link circuit shown in Figure 12b. Then, the plant transfer function employed for tuning the controller is:

$$\frac{V_{dc}(s)}{I_{o\varphi}(s)} = \left(\frac{\beta R_{dc}}{1 + R_{dc}C_{dc}s}\right) \tag{34}$$

With these considerations, the average DC-link voltage control diagram is shown in Figure 13. The notch-filter $H_{NF}(s)$, centered at $2\omega_g = 2\pi(120)$ rad/s, is implemented with the aim of increasing the bandwidth of the PI controller [8]. For this model, it is required that the function $\sin(\varphi)$ in (11) does not present low-frequency variations. Then, if necessary, it is possible to add another notch-filter on the control signal $I_{o\varphi}$. Nevertheless, consider that notch-filter limit the bandwidth of the PI controller to be less than $2\omega_g$.

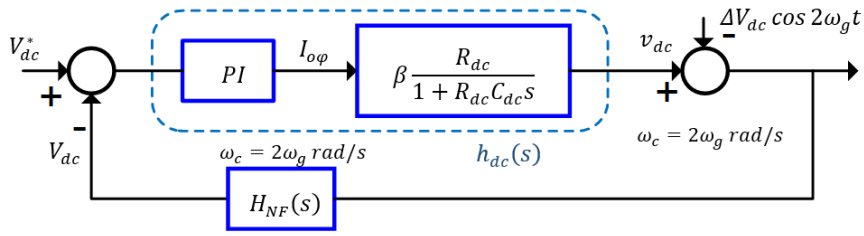

Figure 13. Simplified control block diagram of the average DC-link voltage control.

According to Figure 13 the open-loop transfer function of the system is:

$$h_{dc}(s) = k_p\left(\frac{1 + T_i s}{T_i s}\right)\left(\frac{\beta R_{dc}}{1 + R_{dc}C_{dc}s}\right), \tag{35}$$

The controller gains k_p and $k_i = k_p/T_i$ are determined by performing a zero-pole elimination to establish a chosen cut-off frequency of $\omega_{c,dc}$. Two criteria are used to select the cut-off frequency $\omega_{c,dc}$: inferiorly, to avoid interfering with transient stability, it must be much larger than the power control bandwidth BW_P, since it is the loop with the slowest dynamics; and superiorly, due to the component $2\omega_g$ being canceled by the notch-filter, it must be much smaller than the subsequent harmonic, $4\omega_g$. Hence, a proper relationship is achieved when:

$$5BW_P \leq \omega_{c,dc} \leq (4\omega_g)/5 \tag{36}$$

In the presented control strategy, it has been considered that $\omega_{c,dc} = 6\ BW_P$. Finally, since $I_{o\varphi}$ is linked to the PS φ according to (11), the control signal φ is calculated as:

$$\varphi = \sin^{-1}\left(\frac{I_{o\varphi}}{K_o}\right) \tag{37}$$

In Figure 14 the open-loop frequency response is presented. The controller parameters are summarized in Table 3.

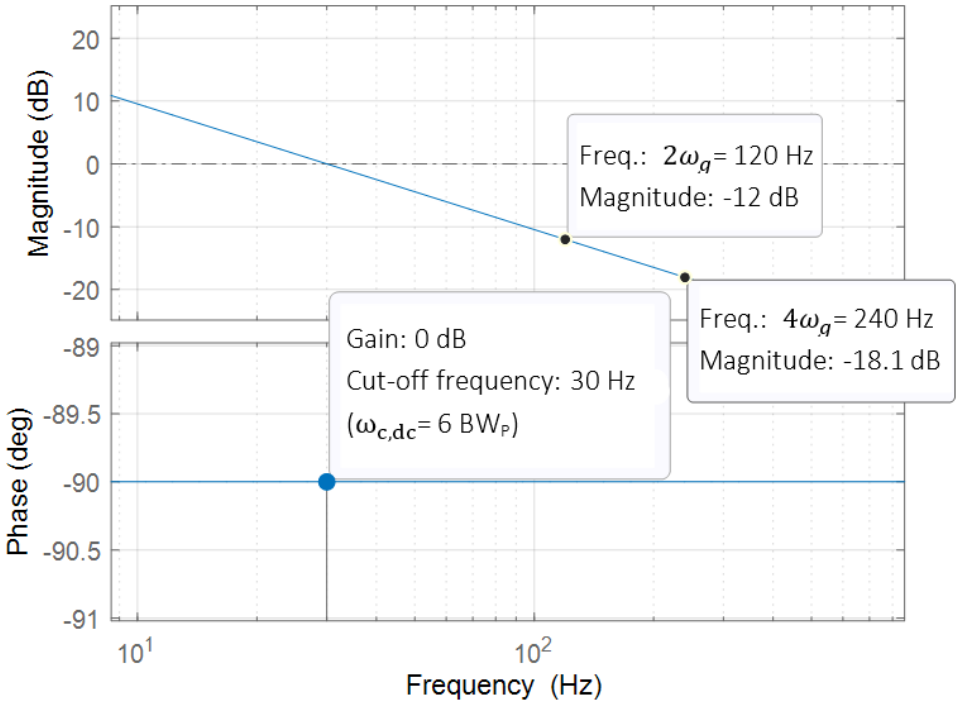

Figure 14. Bode diagram of V_{dc} control open-loop transfer function.

Table 3. Controller parameters.

Symbol	Quantity	Value
k_{pc}, k_r, k_{3r}	PRR current controller gains	1.56, 58.7, 176.2
k_{pv}, k_{rv}	PR voltage controller gains	0.456, 324.2
r_v, x_v	Virtual resistance and reactance	0.33, 0.066
r_{vd}, $\omega_{c,HPF}$	TVR and cut-off frequency	0.3, 75.4 rad/s
k_ω, k_V	Frequency and amplitude droop gains	4%, 10%
H, k_p	Inertia constant and damping factor	0.3452, 0.0530
k_{pq}, k_{iq}	Reactive power controller gains	0.0324, 2.2594
k_p, k_i	DC-link voltage controller gains	0.0452, 1.8617
BW_P	APC bandwidth	$2\pi(5)$ rad/s
BW_{dc}	DC-link voltage control bandwidth	$2\pi(30)$ rad/s

5. Experimental Results Using Hardware-in-the-Loop

Experimental tests have been realized using Typhoon Hardware-in-the-Loop (HIL) 402 to emulate the electronic power circuit in real time, whereas the control was performed by Texas Instruments DSP F28335. The signals used in the control are scaled for digital processing before entering the ADC, whereas the internal control signals are scaled in a 12-bit DAC to have a good resolution when displayed on the oscilloscope. In summary, the scales of the signals shown in the graphs are presented in Table 4.

Table 4. Units and scales of signals plotted in oscilloscope.

Symbol	Value
p_o^*, p_o, q_o	1 p.u./V
Δf_{pcc}, Δf_g	0.1 Hz/V
v_{dc}, Δv_{dc}	100 V/V
v_{ihf}, v_{ohf}	100 V/V
i_{ohf}	3 A/V
I_i	2 A/V
i_o	3.2141 A/V

In Table 4, the scale 0.1 Hz/1V, for example, means that 1V ion the oscilloscope screen represents 0.1 Hz in real signal, and in the same way for the other signals.

5.1. Dynamic Response to Frequency Events

The transient response of active power, reactive power, and frequency of the designed system is shown in Figure 15, where p_o^*, p_o, and q_o are the signals employed in the control presented in Section 3, and Δf_{pcc} is the frequency deviation (in Hertz) in the PCC. It can be seen that p_o develops a damped dynamic with 20% overshoot at the transitions from 0 p.u. to 1 p.u, in V2G operation, with a settling time of approximately 350 ms. Grid-to-vehicle (G2V) operation shows a more damped response with no overshoot and faster settling of around 250 ms since G2V mode has a different dynamic behavior than V2G mode [7]. It can be noticed there is no interference in the transient dynamics of p_o and q_o, since the power control bandwidth is distanced six times with respect to the DC-link voltage control.

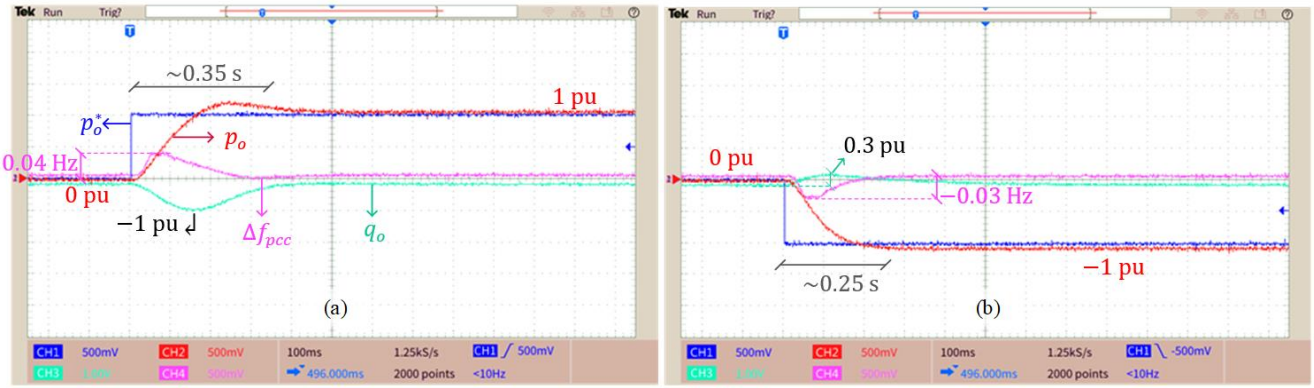

Figure 15. Response of p_o, q_o and Δf_{pcc} to a 100% step for (**a**) V2G, and (**b**) G2V operation.

On the other hand, frequency support and inertial response are tested in Figure 16, operating bidirectionally for events of step variations in the grid frequency Δf_g, and such frequency events can be realized by the advantage provided by the HIL device. Delivering power to the grid at 80% of nominal power, a step down of 0.5 Hz in grid frequency is tested, increasing the output power to its nominal value according to the 4% frequency droop gain with no overshoot and an approximate settling time of 150 ms. In the opposite direction, charging the battery at 80% of the nominal power, the step up of 0.5 Hz in grid frequency forces the battery to be charged at an extra 20% of power.

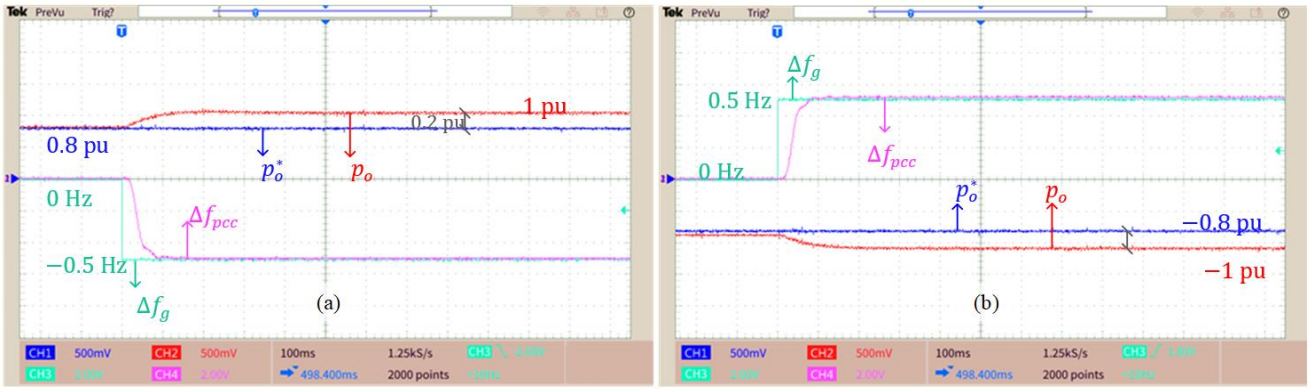

Figure 16. Active power support in cases of grid frequency deviation of: (**a**) 0.5 Hz step down operating at 0.8 p.u., and (**b**) −0.5 Hz step up operating at −0.8 p.u.

Reactive power support for amplitude deviations in the grid voltage are tested in Figure 17. On the left is the case of a 10% increase in the amplitude of the network voltage V_g, forcing the absorption of 1 p.u. of reactive power by the converter according to the 10% voltage droop gain. Conversely, on the right, the case of a 10% decrease in the amplitude forces the injection of 1 p.u. of reactive power to support the grid.

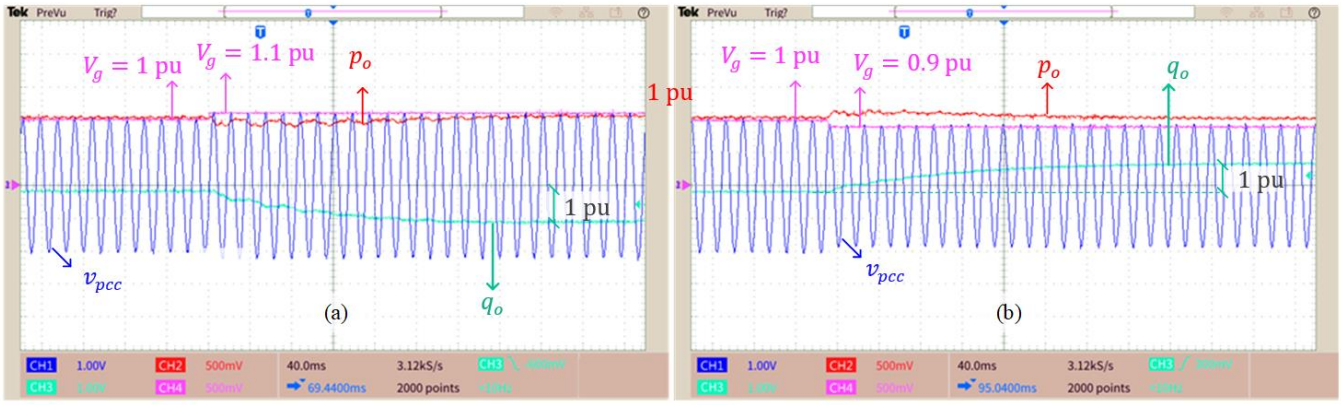

Figure 17. Reactive power support in cases of grid voltage amplitude deviation of: (**a**) 10% step up, and (**b**) 10% step down.

Figure 18 displays the transition from open circuit to full load that occurs when a load of 100% (24.2 Ω) is connected at the output of the converter operating in islanded mode (stand-alone V2H mode). The transient response is faster than grid-tied operation as expected due to the missing of grid line impedance [30], with a settling time of 200 ms. To operate within the normal operating frequency band for small power systems, as mentioned in the network codes of Australia, China, or Great Britain [50], where a maximum frequency deviation of ±0.5 Hz is allowed, for this stand-alone test the frequency droop gain is reduced to $k_\omega = 0.83\%$ to get a maximum frequency deviation of 0.5 Hz if the difference between generation and demand is 1 p.u. However, it can be noted that for this test, the frequency reaches a minimum point of 48.5 Hz momentarily. Moreover, the frequency droop gain can be reduced if the maximum frequency deviation is ±0.2 Hz, as in the European grid code [50]. Note that before load connection, the stability of the system relies on the active damping strategies implemented in the control system.

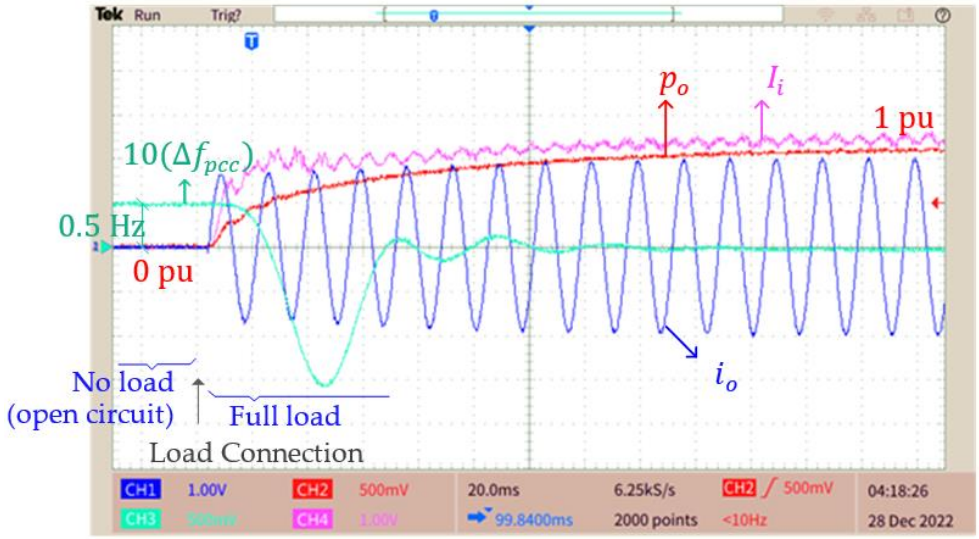

Figure 18. Islanded operation to provide stand-alone services in full load range considering a maximum frequency deviation of ±0.5 Hz.

5.2. Power Decoupling Capability

The responses of the DC-link voltage with DC coupling (v_{dc}, red signal) and AC coupling (Δv_{dc}, cyan signal) to a unit step in the reference power are shown in Figure 19a,b for DC-link capacitors of 240 µF and 120 µF, respectively, for testing the robustness of the designed system. Since in the second case the DC-link capacitor is halved, the PI gains change to maintain a bandwidth $\omega_{c,dc} = 2\pi(30)$ rad/s, while the DC-link ripple increases to double due to the DC-link film capacitor being reduced by half. The DC bus voltage stabilizes smoothly with an approximate settling time of 320 ms, in the presence of high LFR, as in Figure 19a, and very high LFR, as in Figure 19b. Since both tests are designed for the same bandwidth, the settling times are similar.

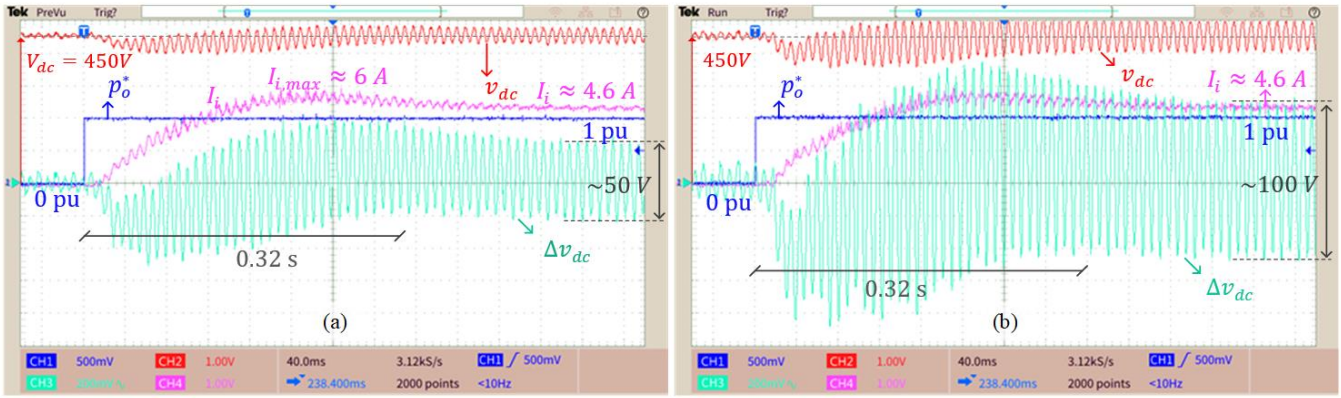

Figure 19. Transient response in the battery current (I_i), DC-link (v_{dc} and Δv_{dc})for unit step in p_o^*. Comparison for C_{dc}: (**a**) 240 µF and (**b**) 120 µF, critical case.

To illustrate the advantage of using the APD algorithm, the steady-state performance at nominal power using two different capacitors in the DC-link is compared in Figure 20. For the first case, the film capacitor of 240 µF, and hence a high LFR ripple, is presented in the DC-link voltage. Meanwhile, the APD is performed by varying the DR angle α_o according to (27) to decouple the single-phase power ripple. For the second case, an electrolytic capacitor of 1.2 mF is used, hence small LFR is presented in the DC-link, and the APD is removed, being $\alpha_o = \pi/2$.

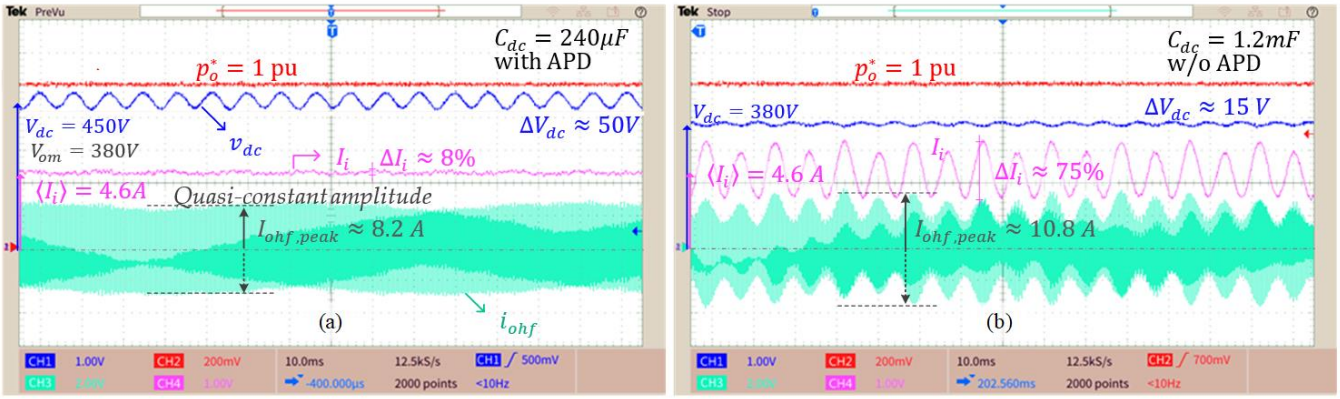

Figure 20. Comparison in I_i and i_{ohf} envelope (**a**) Using APD algorithm with $C_{dc} = 240$ µF, (**b**) Removing APD, only passive decoupling with $C_{dc} = 1.2$ mF. Both with the same HF transformer and series-resonant circuit.

Note in Figure 20a that the high DC-link voltage ripple ΔV_{dc} is allowed to use a small film capacitor, but due to the APD the DC current I_i and envelope amplitude of the HF current i_{ohf} is quasi-constant. Because of the high DC-link ripple $\Delta V_{dc} = 50$ V, the average DC-link voltage is controlled to $V_{dc} = 450$ V, and the APD is performed by the DR angle α_o with the aim of obtaining $V_{om} = 380$ V for the resonant circuit, as presented in Figure 11. Conversely, in Figure 20b, the average DC-link voltage is controlled to $V_{dc} = 380$ V with passive decoupling performed by a large DC-link capacitor, which is $\Delta V_{dc} = 15$ V small. Hence, according to (6) and (12), the series-resonant circuit and the HF transformer are identical for both cases. The PI controller would change according to the average DC link voltage and the DC-link capacitor. As a consequence, it is possible to compare their HF series-resonant circuit and battery currents, i_{ohf} and I_i, for both converters.

In Figure 20, for both cases the rated value of the average battery current $\langle I_i \rangle$ is 4.6 A. For the film capacitor ($C_{dc} = 240$ µF) the peak-to-peak ripple in the battery current is $\Delta I_i \approx 0.4$ A, which is 8.7% of the rated average value. However, for the electrolytic capacitor ($C_{dc} = 1.2$ mF) $\Delta I_i \approx 3.5$ A, which is 75% of rated average value.

From Figure 20a, the peak value of the HF current is $I_{ohf,pk} \approx 8.2$ A, which is near to the expected value $I_{ohf,pk} = 8.5$ A calculated by (29). In comparison, in Figure 20b the HF current gets a peak value $I_{ohf,pk} = 10.8$ A. For the same DABSR design, the film capacitor with APD brings 5.2 A less peak-to-peak HF current than the electrolytic capacitor without APD, which implies reducing not only the DC-link capacitor volume but also the HF transformer and the resonant tank inductor volumes. Furthermore, in terms of electrical performance and lifetime, the film capacitor ($C_{dc} = 240$ µF) offers better characteristics than the electrolytic capacitors. It can be concluded that the proposed APD presents a notable performance, decreasing the HF current amplitude as well as the LFR on the DC current, and shows a better performance than the passive decoupling of an electrolytic capacitor with five times higher capacitance.

The ZVS mode is analyzed operating at nominal power in Figure 21, where high frequency AC voltages, produced by actives bridges, and the tank current are shown. For the V2G direction, ZVS is fulfilled in both active bridges according to the ZVS condition presented in (38). However, for the battery charging direction, ZVS mode can be lost in one leg if the DR angle α_o takes small values.

$$\begin{cases} i_{ohf} > 0; & \omega_s t = \frac{\pi}{2} - \frac{\alpha_o}{2} \\ i_{ohf} < 0; & \omega_s t = \varphi \end{cases} \tag{38}$$

From the graphical results of Figure 21, a phase shift $\varphi \approx 27^\circ$ is measured, which agrees with the estimated phase shift based on the calculation using (30).

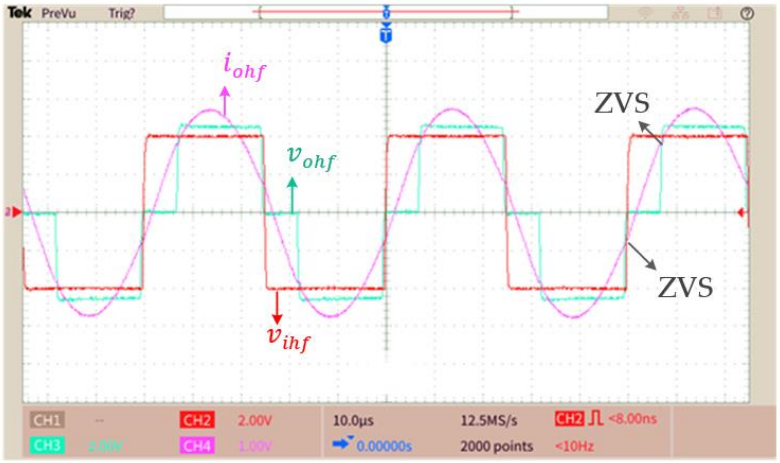

Figure 21. DC-DC ZVS at nominal power operating in V2G.

6. Comparison with Previous Works

With the aim of comparing the GFM and the GFO performances with respect to the THD in the current injected into the grid, the GFO control strategy presented in [20] was set up using the same power circuit presented in Figure 2 to compare using simulation software. For both cases, the analysis has been done using a critical film capacitor $C_{dc} = 120$ µF in the DC-link. For its current controller, a multi-resonant controller P+R_1+R_3 is also implemented, like the inner current control loop presented in Figure 4.

Comparing Figure 22a with Figure 22b, it can be noticed that the THD of the current injected to the grids is quite similar, near to 1.8%. Note that the harmonics distributions are quite different between both control strategies. This is because in a GFO control the grid current reference comes from the v_{dc} control loop [8], unlike the GFM control where the grid current reference comes filtered from the virtual impedance and the low-frequency power loop.

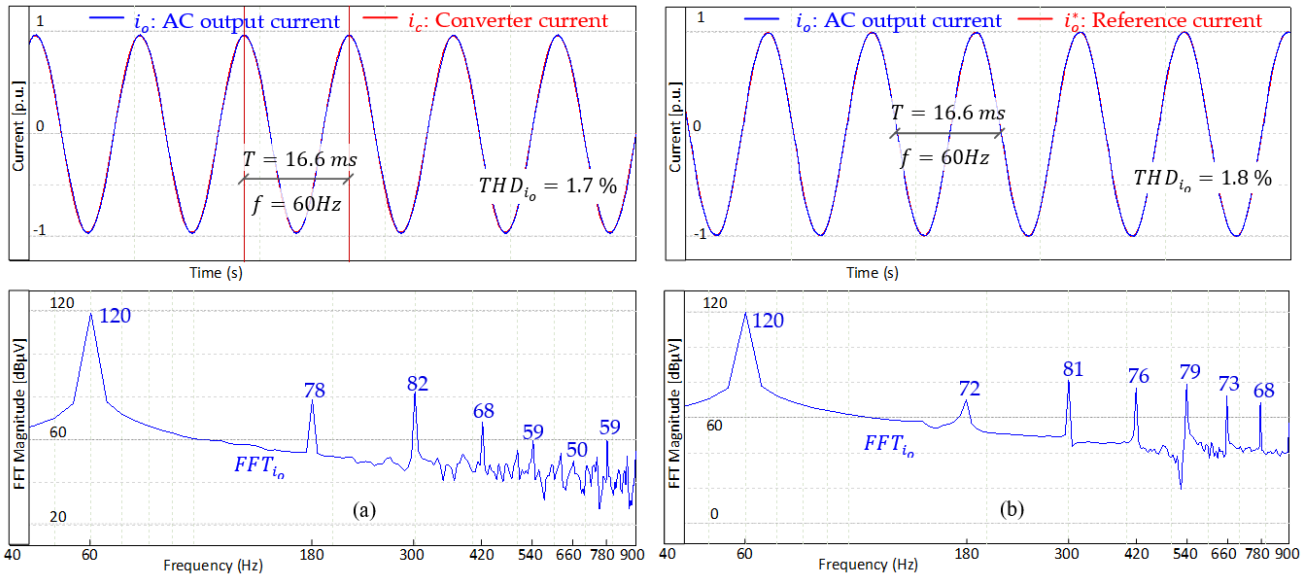

Figure 22. AC output current i_o in time and frequency comparison using identical power circuit with different control strategies: (**a**) Proposed GFM and (**b**) GFO control strategy from [20].

Therefore, it is shown that the GFM strategy can be implemented in a two-stage DC-AC with high ripple in the DC-link, obtaining similar grid current performances than GFO control strategies. The results obtained are relevant because it is known that the GFM control strategies performs better in weak grid conditions [25] and, due to their behave as

controlled voltage sources, they can operate stand-alone to provide V2H services, unlike the GFO control strategies which behave like controlled current sources [27].

Finally, with the aim of highlighting the proposed converter and control strategy for SBC, a brief comparison with other DC-AC structures is presented in Table 5.

Table 5. Proposed converter comparison with others two-stage DC-AC converter.

Parameters	Proposed Converter	Non-Isolated DC-AC [2]	Isolated DC-AC [7]	Isolated DC-AC [20]	Isolated DC-AC [22]
Structure	DC-DC DABSR + VSI	Bidirectional Boost + VSI	DC-DC DAB + VSI	DC-DC DABSR + VSI	DC-DC Three-phase DAB + VSI
DC-Link Capacitor	Film	Electrolytic	Electrolytic	Film	Film
DC-Link Ripple	High (10%)	Low (3%)	Low (3%)	High (10%)	High (10%)
Galvanic Isolation	Yes	Non	Yes	Yes	Yes
Durability	High	Low	Low	High	High
Control Strategy	V2G and Stand-Alone V2H in Unified GFM strategy	V2G (GFO), Stand-Alone AC Voltage Control (V2H)	Only active power V2G Reported (GFO)	Only active power V2G Reported (GFO)	Only stand-alone AC voltage control reported

In [2], a control strategy for SBC is presented using a DC-DC composed of a bidirectional Boost converter DC-linked by electrolytic capacitors with a VSI. For this structure, V2G and stand-alone V2H have been reported in the literature. However, it does not have galvanic isolation and suffers from limited durability due to the use of electrolytic capacitors. Galvanic isolation is added used a DC-DC DAB in [7]. However, it has the same drawback of having limited durability by the usage of electrolytic capacitors in the DC-link. With the aim of increasing the converter durability, a similar structure of the proposed converter, using film capacitors in the DC-link, is presented in [20]. However only active power support for V2G services is reported. This structure has the drawback of having the double control loop DC-link voltage–grid current for the VSI, which can increase the THD in the grid current, since the grid current reference comes from the DC-link voltage loop, which has a high DC-link ripple [8]. Finally, a two-stage DC-AC converter with a different isolated DC-DC structure is presented in [22] for fuel cell applications, but only stand-alone control is presented. Therefore, with the previous comparison, the proposed DC-AC converter is a good candidate for single-phase SBC, because it integrates V2G and stand-alone V2H capability in a unified GFM control strategy that offers high-quality power in its terminals, with the additional advantages of having galvanic isolation and high durability.

7. Conclusions

In this paper, a PLL-free single-phase GFM control strategy with active power decoupling for an isolated and bidirectional two-stage DC-AC converter considering high DC-link voltage ripple due to the use of film capacitors is presented. For a simplified tuning of the controllers, a distinction is made between low, medium, and high-speed controllers. The single-phase GFM control is tuned to operate with damped behavior against strong ripple from the DC link and low damping situations, such as when feeding small loads in stand-alone mode and avoiding the bandwidth coupling between their loops and with the DC-DC control. The active power decoupling, galvanic isolation, and soft switching features are combined with the grid forming characteristic to bring V2G and stand-alone V2H services. The proposed GFM strategy, average DC-link voltage control, and active power decoupling have been validated for grid events and stand-alone operation. The grid current of the proposed single-phase GFM control has been compared with an equivalent GFO control using the same power circuit. Results show that similar performances in the

grid current THD are obtained. The results obtained are relevant because it is known that the GFM control strategies perform better in weak grid conditions and can operate stand-alone to provide V2H services, unlike the GFO control strategies. On the other hand, the proposed APD along with the average DC-link voltage control has been validated for different capacitance values in the DC-link. Results show that the proposed APD suppresses the LFR in the battery current as well as reduces the HF tank current amplitude in comparison with the typical passive power decoupling using electrolytic capacitors. ZVS mode is obtained by allowing high efficiency in the DABSR DC-DC converter. The proposed control strategy has been compared with similar structures, showing better features. Hence, the proposed converter along with the single-phase GFM strategy can be implemented in SBCs for V2G and stand-alone V2H applications. Finally, it is important to highlight that the proposed converter may work for unbalanced three-phase systems, which will be validated in future works.

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